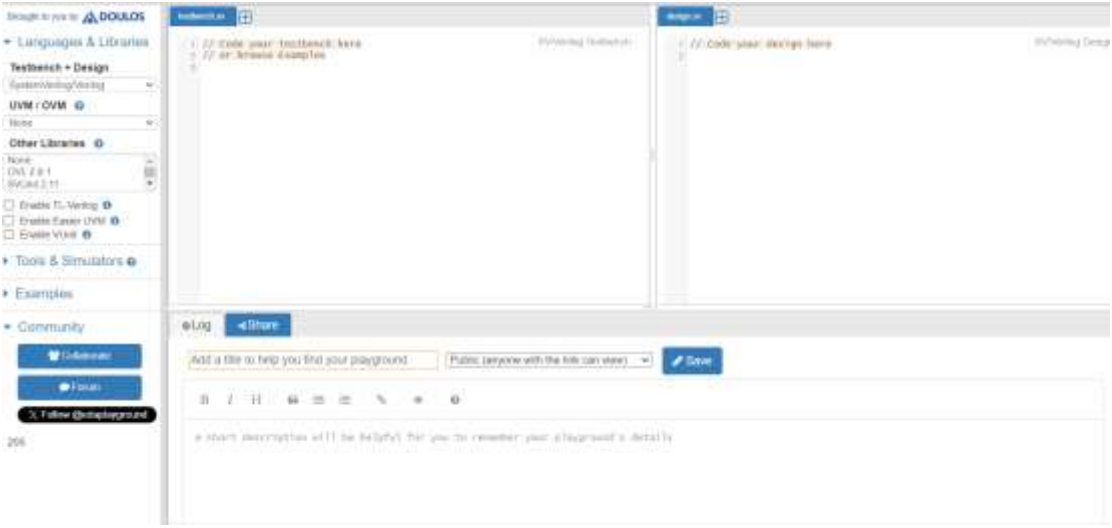
第 1 講 edaplayground 平台使用

1. 參考文獻:
   - Online Verilog Simulator: edaplayground 教學: https://www.youtube.com/watch?v=f9uwtAax4v0&t=249s
   - 金門大學陳鍾誠老師電子書: http://ccckmit.wikidot.com/ve:main

2. edaplayground: https://www.edaplayground.com/
   - 介面

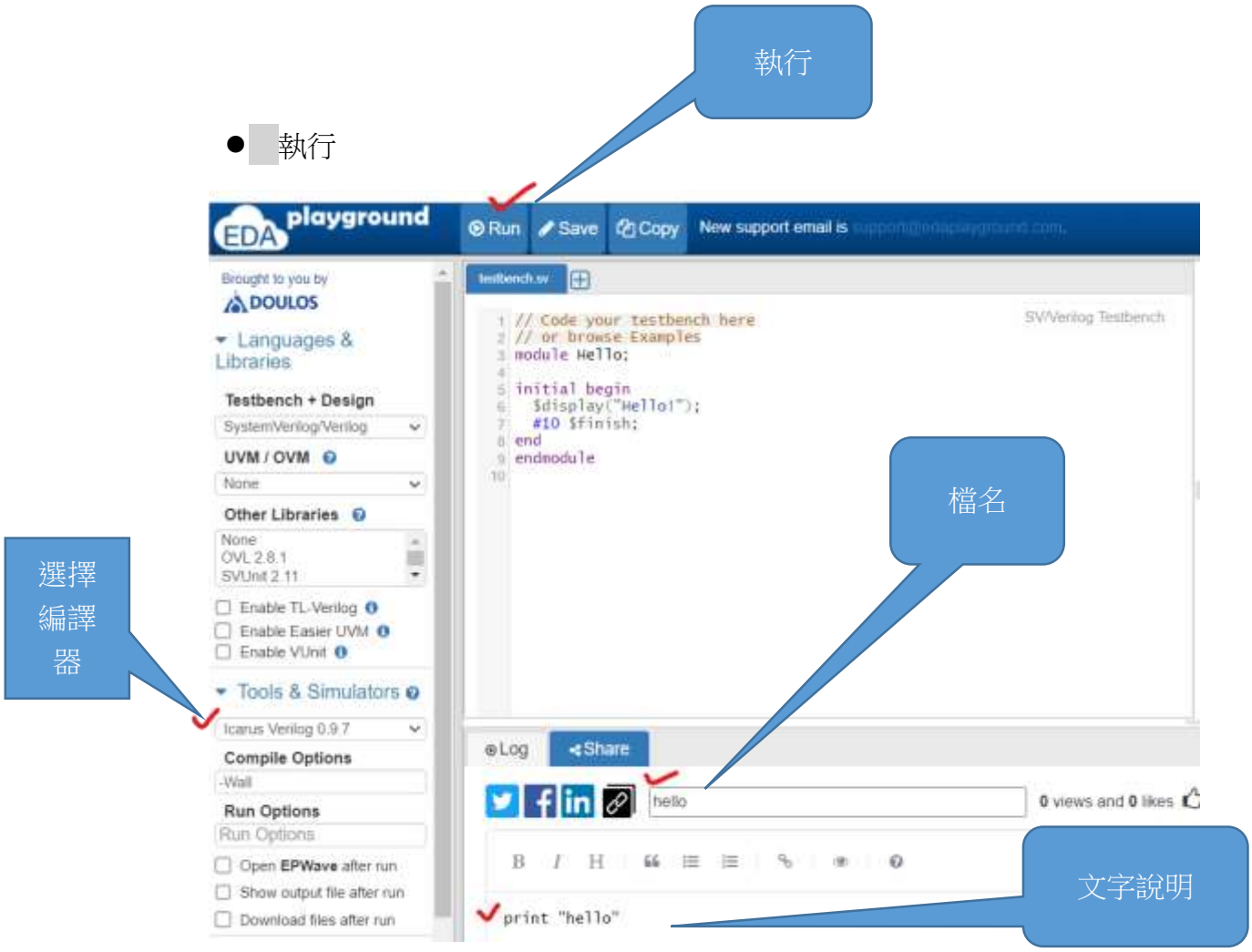


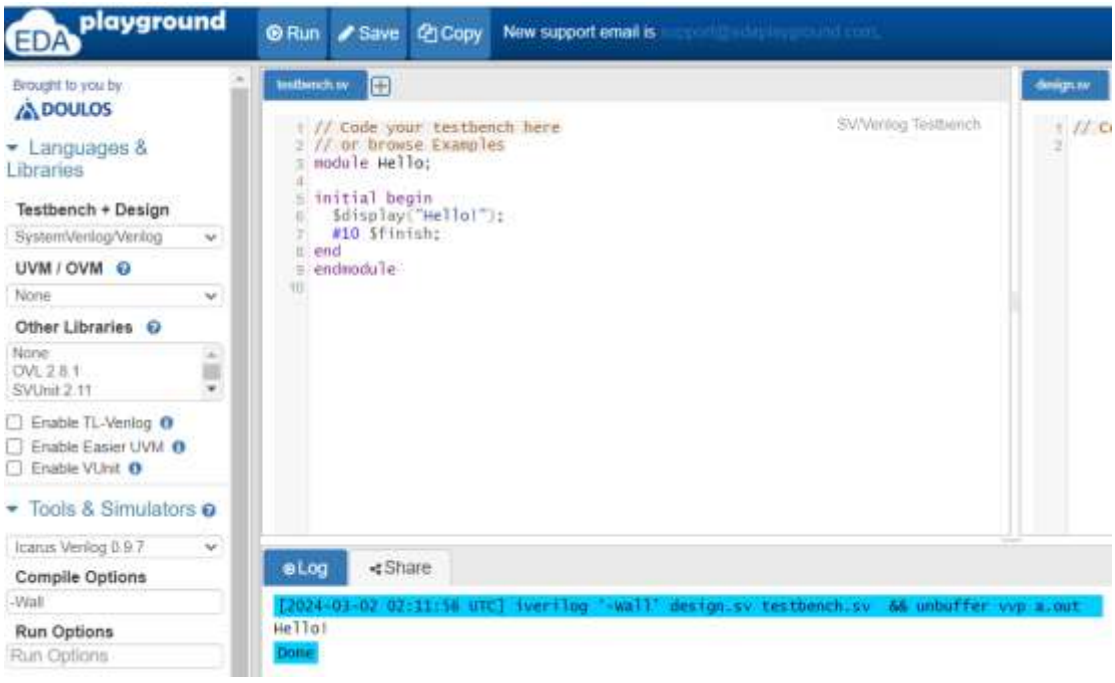
例題 1: Hello

```
module Hello;
initial begin
  $display("Hello!");
  #10 $finish;
end
endmodule
```

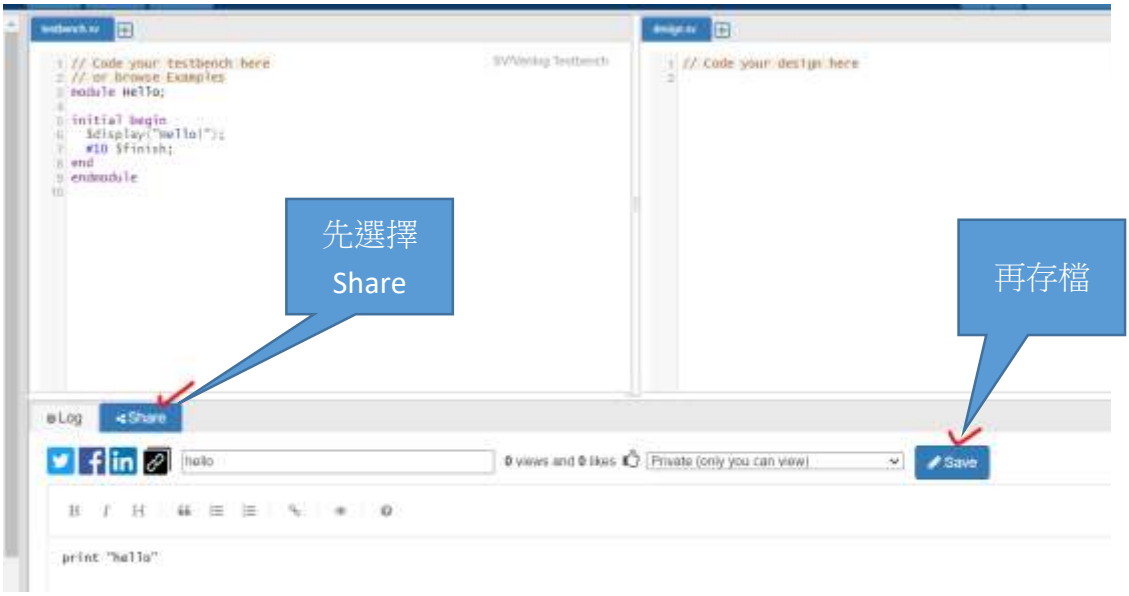
複製例題 1 內容， 貼到 “testbench.sv”，如下圖

- 執行

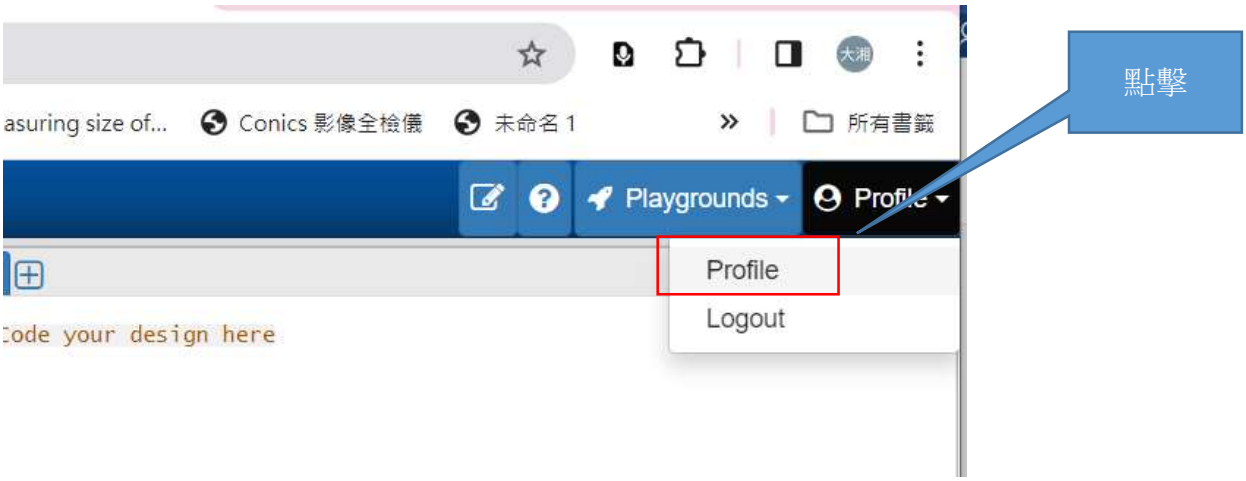

執行
playground
Run
Save
Copy
New support email is
Brought to you by
DOULOS
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Icarus Verilog 0.9.7
Compile Options
-Wall
Run Options
Run Options
Open EPWave after run
Show output file after run
Download files after run
testbench.sv
SV/Verilog Testbench
// Code your testbench here
// or browse Examples
module Hello;
initial begin
$display("Hello!");
#10 $finish;
end
endmodule
檔名
選擇編譯器
Log
Share
hello
0 views and 0 likes
print "hello"
文字說明


playground
Run
Save
Copy
New support email is
Brought to you by
DOULOS
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Icarus Verilog 0.9.7
Compile Options
-Wall
Run Options
Run Options
testbench.sv
design.sv
SV/Verilog Testbench
// Code your testbench here
// or browse Examples
module Hello;
initial begin
$display("Hello!");
#10 $finish;
end
endmodule
Log
Share
[2024-03-02 02:11:58 UTC] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
Hello!
Done

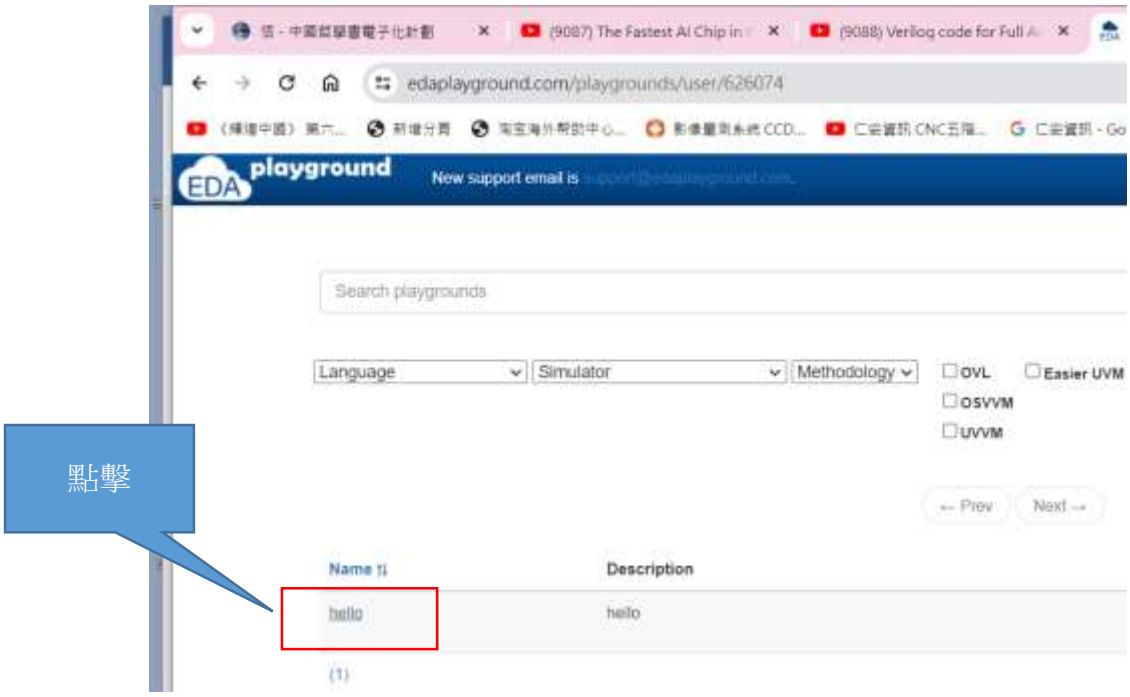
- 存檔


先選擇
Share
再存檔
Log
Share
hello
0 views and 0 likes
Private (only you can view)
Save
print "hello"

- 雲端取檔


點擊
asuring size of...
Conics 影像全檢儀
未命名 1
所有書籤
Playgrounds
Profile
Profile
Logout
Code your design here


點擊
edaplayground.com/user/626074
playground
New support email is
Your Playgrounds
Published Playgrounds
User Pr
Your Details



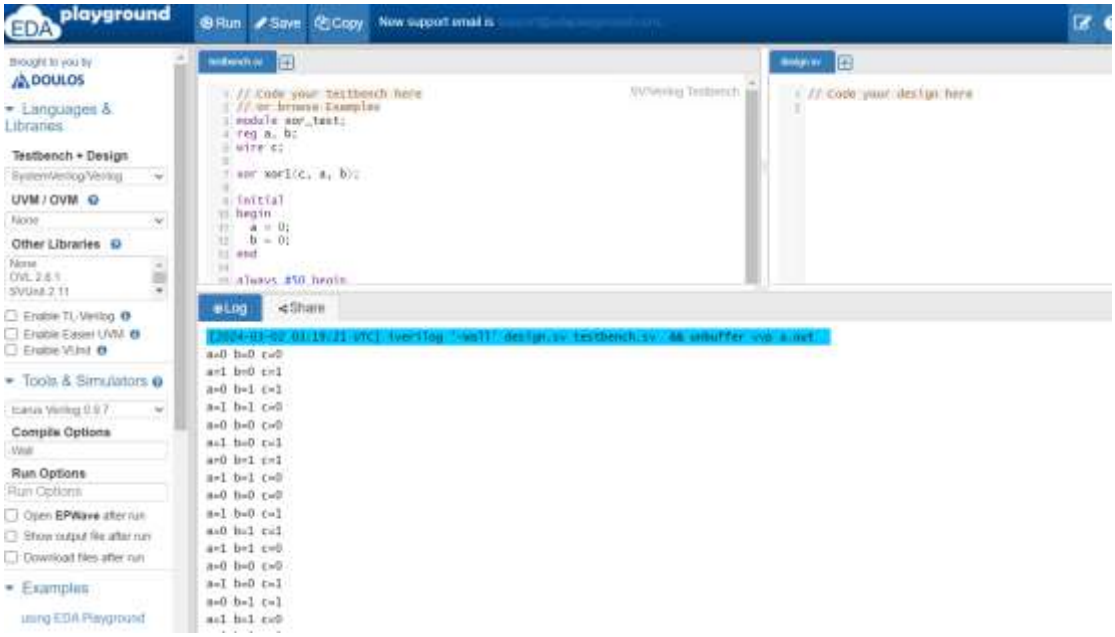
隨後取回“hello.sv”檔案

例題 2. xor

```
module xor_test;
reg a, b;
wire c;

xor xor1(c, a, b);

initial
begin
  a = 0;
  b = 0;
end

always #50 begin
  a = a+1;
end

always #100 begin
  b = b+1;
end
```

```
always @(a or b) begin
  $display("a=%d b=%d c=%d", a, b, c);
end

initial #2000 $finish;

endmodule
```

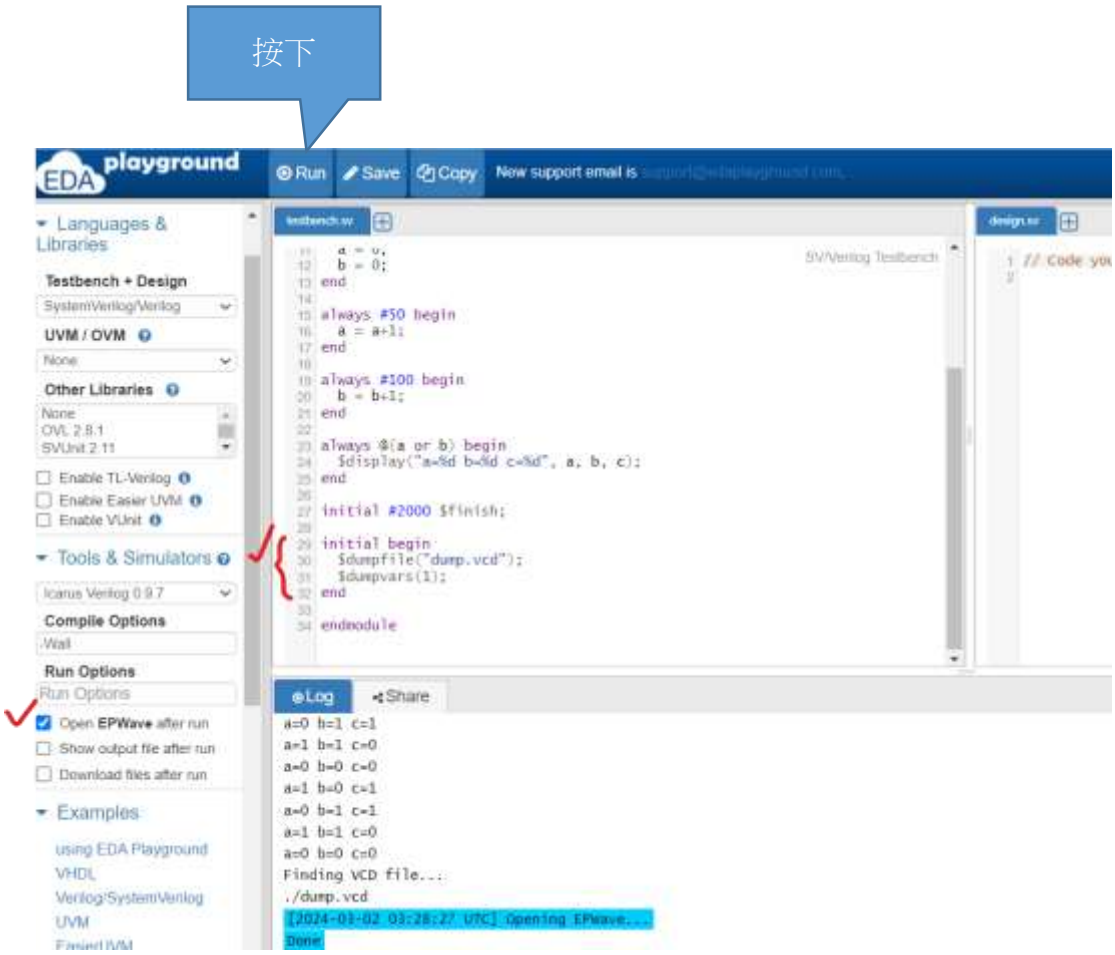
複製例題 2 內容， 貼到“testbench.sv”如下圖，並執行



使用圖形顯示，加上以下文字，

```
initial begin
   $dumpfile("dump.vcd");
   $dumpvars(1);
end
```

並勾選 Open EPwaves after run 選項後按下 run，如下圖所示，


按下
playground
Run
Save
Copy
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Icarus Verilog 0.9.7
Compile Options
-Wall
Run Options
Run Options
Open EPWave after run
Show output file after run
Download files after run
Examples
using EDA Playground
VHDL
Verilog/SystemVerilog
UVM
testbench.sv
design.sv
SV/Verilog Testbench
a = 0;
b = 0;
end
always #50 begin
a = a+1;
end
always #100 begin
b = b+1;
end
always @(a or b) begin
$display("a=%d b=%d c=%d", a, b, c);
end
initial #2000 $finish;
initial begin
$dumpfile("dump.vcd");
$dumpvars(1);
end
endmodule
// Code yo
Log
Share
a=0 b=1 c=1
a=1 b=1 c=0
a=0 b=0 c=0
a=1 b=0 c=1
a=0 b=1 c=1
a=1 b=1 c=0
a=0 b=0 c=0
Finding VCD file...
./dump.vcd
[2024-03-02 03:28:27 UTC] Opening EPWave...
Done


playground
Run
Save
Copy
Playgrounds
EPWave
From:
To:
Get Signals
Radix
100%
135s

作業 1-1: 4 bit adder

```
module fulladder (input a, b, c_in, output sum, c_out);
wire s1, c1, c2;

xor g1(s1, a, b);
xor g2(sum, s1, c_in);
and g3(c1, a,b);
and g4(c2, s1, c_in) ;
xor g5(c_out, c2, c1) ;

endmodule

module adder4(input signed [3:0] a, input signed [3:0] b,
input c_in, output signed [3:0] sum, output c_out);
wire [3:0] c;

fulladder fa1(a[0],b[0], c_in, sum[0], c[1]) ;
fulladder fa2(a[1],b[1], c[1], sum[1], c[2]) ;
fulladder fa3(a[2],b[2], c[2], sum[2], c[3]) ;
fulladder fa4(a[3],b[3], c[3], sum[3], c_out) ;

endmodule
```

以上請複製貼上網頁 edaplayground 右側 “design.sv”

以下文字請複製貼上 左側 “testbench.sv”

```
//testbench
module main;
reg signed [3:0] a;
reg signed [3:0] b;
wire signed [3:0] sum;
wire c_out;

adder4 DUT (a, b, 1'b0, sum, c_out);
```

```
initial
begin
  a = 4'b0101;
  b = 4'b0000;
end

always #50 begin
  b=b+1;
  $monitor("%dns monitor: a=%d b=%d sum=%d", $stime, a, b,
sum);
end

initial #1000 $finish;

endmodule
```

(1) 請執行上述程式，將結果貼到作業報告中，
(2) 若要產生輸出波形，請問應如何修改，並將結果貼到作業報告中。